REMARKS

Claims 1-17, all the claims pending in the application, stand rejected upon informalities and on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. Claim Objections

Claims 3, 9, and 14 were objected to under 37 CFR §1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Independent claims 1, 7, and 13, from which claims 3, 9, and 14, respectively, depend are amended herein so that claims 3, 9, and 14 are now in proper dependent form. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objections to claims 3, 9, and 14 under 37 CFR 1.75(c).

II. The 35 U.S.C. §112, Second Paragraph, Rejection

Claims 1-17 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. The Applicants respectfully traverse these rejections.

Paragraph [0026] of the specification provides that "the invention can utilize the fins [i.e., fins having different gate dielectric thicknesses] in many different types of transistors. For example, the invention can form complementary transistors on the same substrate, or can form transistors with different voltage requirements on different areas of the substrate. Therefore, in these situations, certain types of transistor would include gate

dielectrics having a first thickness and other types of transistor could include gate dielectrics having a second thickness. Also, the invention can utilize the fins in multiple-fin transistors". Independent claims 1 and 7 are amended herein to reflect that the claimed invention is for "a semiconductor structure having at least one fin-type field effect transistor (FinFET)".

In order to further clarify the subject matter of the claimed inventions, independent claims 1 and 7 are amended herein to reflect that the claimed invention is for "a semiconductor structure having at least one fin-type field effect transistor (FinFET)". Additionally, independent claim 13 is amended herein to reflect that the claimed invention is for "a semiconductor structure having multiple fin-type field effect transistors". Claims 2 and 8 (which depend from claims 1 and 7, respectively), as well as independent claim 13, reflect an embodiment in which the "fins are utilized in different types of transistors on said substrate". Thus, as indicated in paragraph [0026], each fin can be utilized in a different type of FinFET on the substrate. Whereas claims 3 and 9 (which also depend from claims 1 and 7, respectively) reflect an embodiment in which the "fins are utilized in at least one multiple-fin transistor". Thus, as indicated in paragraph [0026], each fin can be utilized in multiple-fin transistors (i.e., either the same or different multiple-fin transistors). Claim 14, which depends from claim 13, further limits claim 13 by providing that the "fins are utilized in multiple-fin transistors". Therefore, as amended, the claims particularly point out and distinctly claim the subject matter of the invention and the Examiner is respectfully requested to reconsider and withdraw rejections of claims 1-17 under 35 U.S.C. §112.

III. The Prior Art Rejections

The Office Action provided alternative prior art rejections based on two different interpretations of the claimed invention. Specifically, the Office Action indicated that if the claimed invention were for "a plurality of transistors", the following rejections apply: (1) Claims 1-2, 4, 7-8, 10, 13 and 15 stand rejected under 35 U.S.C. §102(e) as being anticipated by Chau, et al., (U.S. Patent No. 6,858,478), hereinafter referred to as Chau; and (2) Claims 3, 5, 6, 9, 11, 12, 14, 16 and 17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over a combination of Chau, Hu, et al. (U.S. Patent No. 6,413,802, hereinafter referred to as Hu), and Ahmed, et al. (U.S. Patent No. 6,787,439, hereinafter referred to as Ahmed). Alternatively, the Office Action indicated that if the claimed invention were for a single "multiple fin transistor", then the following rejections would apply: (1) Claims 1-4, 7-10, and 13-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over a combination of Chau and Hu; and (2) Claims 5, 6, 11, 12, 16 and 17 stand rejected under 35 U.S.C. §103(a) over a combination of Chau, Hu and Ahmed.

As mentioned above, the invention can utilize the fins, having different gate dielectric thicknesses, in many different types of transistors or in the same or different multiple-fin transistors. The independent claims 1 and 7 broadly claim a semiconductor having at least one FinFET. Claims 2 and 8, which respectively depend from claims 1 and 7, as well as independent claim 13, limit the invention such that each fin can be utilized in a different type of FinFET on the substrate. Claims 3 and 9, which also respectively depend from claims 1 and 7, alternatively, limit the invention such that the fins are utilized in at least one multiple-fin transistor.

Applicants respectfully traverse all of these rejections under 35 U.S.C. §102(e) and/or 35 U.S.C. §103(a) because regardless of whether the fins are utilized in different single-fin transistors on the same substrate or the same or different multiple-fin transistors on the same substrate, neither Chau alone, nor Chau in combination with Hu and/or Ahmed teach or disclose the following feature of independent claims 1, 7 and 13: "gate dielectrics covering said fins, wherein said gate dielectrics have different thicknesses". Furthermore, regarding independent claim 13, neither Chau alone, nor Chau in combination with Hu and/or Ahmend teach or disclose that the "fins are utilized in different types of transistors on said substrate, and wherein a first type of transistor includes gate dielectrics having a first thickness and a second type of transistor includes gate dielectrics having a second thickness different than said first thickness". Lastly, regarding independent claim 7, neither Chau alone, nor Chau in combination with Hu and/or Ahmend teach or disclose that the "fins have different thicknesses".

More particularly, the Office Action cites Figures 7A and 7B of Chau as disclosing a similar device to that of the claimed invention. The Office Action states that "Figures 7A and 7B disclose a fin-type field effect transistor with a fin (702) extending from a substrate (700). The fin (702) has a gate dielectric (712, 714) with different thicknesses. It is understood that a plurality of fins is formed on the substrate (700), each with a gate dielectric having a different thickness." However, the Applicants respectfully submit that the cited figures do not illustrate a plurality of fins with different dielectric thicknesses (as in claims 1 and 3) formed on the same substrate. Similarly, the cited

figures do not illustrate that the "fins are utilized in different types of transistors on said substrate, and wherein a first type of transistor includes gate dielectrics having a first thickness and a second type of transistor includes gate dielectrics having a second thickness different than said first thickness". On the contrary, Figures 7A and 7B of Chau simply disclose two different embodiments of the same invention (a tri-gate device).

The invention of Chau comprises a single tri-gate device (not a FinFET which, as defined by the Hu, is a double gate device with a thin silicon fin (see Abstract and column 2, lines 19-31)). Specifically, Chau teaches an embodiment of a single tri-gate transistor, as illustrated in Figure 7A, comprising a semiconductor body, in which the height is approximately equal to or ½ to 2 times the width (and thus, by definition not a fin), and a dielectric layer on the sidewalls and top surface of the body (see column 13, lines 42-60). Additionally, Chau teaches another embodiment of a single tri-gate transistor, as illustrated in Figure 7B, having a semiconductor body, as described in the above, and a composite dielectric layer on the sidewalls and top surface of the body (see column 13, line 62- column14, lines 1-21). In both of these embodiments the thickness of the gate dielectric layer on the top surface is different from that on the sidewalls of the semiconductor body. Chau further teaches the associated methods of forming one or the other of these different tri-gate transistors on a substrate. However, Chau does not teach or disclose that these two different embodiments can be formed on the same substrate simultaneously. The Applicants respectfully disagree with the assumption in the Office Action that it is "understood that a plurality of fins is formed on the substrate (700) each

with a gate dielectric having different thickness", as no such method is disclosed whereby a plurality of semiconductor bodies with different thicknesses could be formed. Additionally, it is not obvious over Chau how a plurality of semiconductor bodies with different thicknesses would be formed on the same substrate given the significantly different methods that are disclosed by Chau for forming a tri-gate device of Figure 7A (see column 14 line 63-column 15,line 17) and a tri-gate device of Figure 7B (see column 14, lines 22-54).

Lastly, neither Chau alone, nor Chau in combination with Hu and/or Ahmend teach or disclose the feature of claim 7 that the "fins have different thicknesses". Paragraph [0028] of the specification teaches an embodiment of the invention in which not only the gate dielectrics have different thickness, but so do the fins (as a result of the silicon consumption during an oxide growth phase). The Office Action provides that claim 7 is anticipated by Figures 7A and 7B of Chau, but does not particularly address the features of that the "fins have different thicknesses". As mentioned above, Chau discloses various embodiments (i.e., embodiments illustrated in Figures 7A and 7B) of a tri-gate device in which the height of the semiconductor body is approximately equal to (or ½ to 2 times) the width (see column 4, lines 10-18). Again, Chau does not teach or disclose two different transistors with different dielectric thicknesses on the same substrate at the same time, much less two different transistors with two different dielectric thicknesses and different fin thicknesses on the same substrate.

Therefore, independent claims 1, 7 and 13 are patentable over Chau alone, as well as over Chau in combination with Hu and/or Ahmend. Furthermore, dependent claims 2-

6, 8-12 and 14-17 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define.

Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

With respect to both the objections to and the rejections of the claims, the claims have been amended, above, to overcome these objections and rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objections to and rejections of the claims.

In view of the foregoing, Applicants submit that claims 1-17, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 9-8-05

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